FIG. 1

FIG. 3

FIG. 4

FIG. 2A

<Original data string>

B00	B01	B02	B03	· · · · · ·

FIG. 2B

<ECC configuration>

B00	B01	B02	B03	· · · ·	P00	· · ·
B10	B11	B12	B13	· · · ·	P10	· · ·
B20	B21	B22	B23	· · · ·	P20	· · ·
·	·	·	·	· ·	·	·
·	·	·	·	· ·	·	·
·	·	·	·	· ·	·	·
Q00	Q01	Q02	Q03	· · · ·	R00	· · ·
Q10	Q11	Q12	Q13	· · · ·	R10	· · ·

PI

PO

FIG. 2C

<Precoding data string>

B00	B01	B02	B03	· · · · · ·	P00	· · · · · ·	Bn0	Bn1	Bn2	Bn3	· · ·	Pn0	· · ·

FIG. 2D

<Recording data string>

S0	B' 00	B' 01	B' 02	· · · · · ·	S1	B' xx	· · · · · ·

Synchronous frames

FIG.5

FIG.6

FIG.7

2

4

4

A2

A1

Physical segment

B'an   B'bn   B'cn   B'dn

⟨Data segment⟩

Additional synchronous frame

⟨Recorded data⟩

Overlapped part

⟨Additional recording data⟩

Begin additional synchronous frame

End additional frame

F I G. 8

Z_0 zone

Z_1 zone

1

2

3

F I G. 9

5

6

Groove format modulation section

Land format modulation section

FIG. 10

Original
data → | ECC configuration circuit | 15 → | Data segment string creating circuit | 16

| Format detecting circuit | 12
| Data reproducing circuit | 13

Original data

FIG. 11A

Wobble modulation section

Reproduced signal

FIG. 11B

Data segment

FIG. 12

FIG. 13

Binary code	Gray code
000000	000000
000001	000001
000010	000011
000011	000010
000100	000110
000101	000111
000110	001111

First area   Second area   Second area   Third area   Third area

F I G. 14

F I G. 15A

Second area

F I G. 15B   Groove reproduced signal

F I G. 15C   Land reproduced signal

F I G. 16

Wobble synchronous clock generating circuit

Format detecting circuit

Format information

Land-groove decision circuit

F I G. 17

F I G. 18

FIG. 19

(MSB) b31 ... b24 b23 ... b0 (LSB)

Data field information	Data field number

b31 | b30 | b29 | b28 | b27 | b26 b25 | b24

Sector format type	Tracking method	Reflectivity	Recording type	Area type	Data type	Layer number

FIG. 20A

Initial preset number	Initial preset value	Initial preset number	Initial preset value
0h	0001h	8h	0010h
1h	5500h	9h	5000h
2h	0002h	0Ah	0020h
3h	2A00h	0Bh	2001h
4h	0004h	0Ch	0040h
5h	5400h	0Dh	4002h
6h	0008h	0Eh	0080h
7h	2800h	0Fh	0005h

Initial value of shift register

FIG. 20B

r14	r13	r12	r11	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0

Feedback register

← 172 bytes →		PI 10 bytes		← 172 bytes →			PI 10 bytes	
B0,0	B0,171	B0,172	B0,181	B0,182	B0,353	B0,354	B0,363
B1,0	B1,171	B1,172	B1,181	B1,182	B1,353	B1,354	B1,363
B2,0	B2,171	B2,172	B2,181	B2,182	B2,353	B2,354	B2,363
B189,0	B189,171	B189,172	B189,181	B189,182	B189,353	B189,354	B189,363
B190,0	B190,171	B190,172	B190,181	B190,182	B190,353	B190,354	B190,363
B191,0	B191,171	B191,172	B191,181	B191,182	B191,353	B191,354	B191,363
B192,0	B192,171	B192,172	B192,181	B192,182	B192,353	B192,354	B192,363
B207,0	B207,171	B207,172	B207,181	B207,182	B207,353	B207,354	B207,363

192 rows · PO 16 rows

(ECC block structure)

FIG. 21

One scrambled frame

	172	10	172	10
6	0-L		0-R	
	1-R		1-L	
	2-L		2-R	
		PI		PI
	31-R		31-L	
16	PO		PO	

208

(Arrangement of scrambled frames)

FIG. 22

0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	10
11	11
12	12
13	13
14	14
15	15
16	16
17	17
18	18
19	19
20	20
21	21
22	22
23	23
24	24
25	25
26	26
27	27
28	28
29	29
30	30
31	31

12+1
Two
recording
frames

PO
(Line interleaving)

PI

13×16=208

172   10   172   10

F I G. 23

Even-number-recorded data field (F)

	24	1092	24	1092	24	1092	24	1092
	SY0		SY1		SY1		SY1	
	SY2		SY1		SY1		SY3	
	SY1		SY2		SY2		SY1	
	SY3		SY2		SY1		SY2	
	SY3		SY3		SY3		SY2	
	SY2		SY2		SY3		SY2	
	SY3		SY1		SY3		SY2	
	Sync frame		Sync frame		Sync frame		Sync frame	

7 rows

F I G. 24A

Odd-number-recorded data field (F)

	24	1092	24	1092	24	1092	24	1092
	SY1		SY1		SY0		SY1	
	SY1		SY3		SY2		SY1	
	SY2		SY1		SY1		SY2	
	SY1		SY2		SY3		SY2	
	SY3		SY2		SY3		SY3	
	SY3		SY2		SY2		SY2	
					SY3		SY1	
	Sync frame		Sync frame		Sync frame		Sync frame	

7 rows

F I G. 24B

	(MSB)	Primary SYNC codes		(LSB)		(MSB)	Secondary SYNC codes		(LSB)
State0									
SY0	000010	101000	000000	001001	/	000010	001000	000000	001001
SY1	100001	001000	000000	001001	/	100010	101000	000000	001001
SY2	100100	001000	000000	001001	/	101000	101000	000000	001001
SY3	101000	001000	000000	001001	/	101010	001000	000000	001001
State1									
SY0	000100	101000	000000	001001	/	000100	001000	000000	001001
SY1	001001	001000	000000	001001	/	001010	101000	000000	001001
SY2	010000	101000	000000	001001	/	010000	001000	000000	001001
SY3	010100	001000	000000	001001	/	010101	001000	000000	001001

(SYNC code)

F I G. 25

Guard area

Guard area

Data segment format

Guard VFO,PS,etc	ECC block (32 Data frame)	Guard PA,etc

F I G. 26A

Physical segment 0

1	2	3	4	5	6

F I G. 26B

Physical segment format

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

F I G. 26C

Wobble data unit (Primary)

1b	0b	bit 2	bit 1	bit 0	0b
2 wobble	2 wobble	4 wobble	4 wobble	4 wobble	68 wobble

F I G. 26D

Wobble data unit (Secondary for R)

1b	0b	bit 2	bit 1	bit 0	0b
2 wobble	2 wobble	4 wobble	4 wobble	4 wobble	26 wobble

0b
42 wobble

F I G. 26E

(Layout of wobble data unit)

(Primary)

SYNC	1b	0b	1b	0b
	6 wobble	4 wobble	6 wobble	68 wobble

F I G. 27A

Data	1b	0b	bit 2	bit 1	bit 0	0b
	2 wobble		4 wobble	4 wobble	4 wobble	68 wobble

F I G. 27B

monotone	0b
	84 wobble

F I G. 27C

Wobble direction

Outer ← → Inner

0b   1b

F I G. 27D

RAM

SYNC	Segment	Zone	Segment information		Groove Track	Land Track	monotone
3	6	5	6	1	12	12	6

Layer	Reserved
1	5

Parity
1

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

← Wobble data unit

FIG. 28A

R

SYNC	Segment	Segment information	CRC	monotone
3	18	6	12	12

Layer	Reserved
1	5

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

← Wobble data unit

FIG. 28B

SYNC	Segment	Zone	Segment information	Parity	Groove track (m+2)	–	monotone
SYNC	Segment	Zone	Segment information	Parity	–	Land track (m+2)	monotone
SYNC	Segment	Zone	Segment information	Parity	Groove track (m+1)	–	monotone
SYNC	Segment	Zone	Segment information	Parity	–	Land track (m+1)	monotone
SYNC	Segment	Zone	Segment information	Parity	Groove track (m)	–	monotone
SYNC	Segment	Zone	Segment information	Parity	–	Land track (m)	monotone

Outer edge of disk ←

Groove
Land
Groove
Land
Groove
Land

Inner edge of disk →

F I G. 29

F I G. 30

Physical segment (n)

Physical segment (n+1)

Write start point

Guard1
VFO, PS, etc

ECC block (m+1)

0+J

71

77+J+K

31+J+K

40-J-K

6+J+K

22

24

ECC block (m)

Guard2
PA, etc

Guard3

Write end point

Minimum value of Guard 1 properly reproduced   31Byte
Minimum value of Guard 2 properly reproduced   6Byte
Minimum value of overlap to prevent unrecorded parts from being left   8Byte

Random shift
shift value for ECC block (m+1)   J=0~15
shift value for ECC block (m)   K=0~15

F I G. 31

Physical segment (n)   Physical segment (n+1)

ECC block (m+1)

Write start point

Guard1
VFO, PS, etc

71

63

93

8

8

22

22

Guard3

Guard2
PA, etc

Write end point

ECC block (m)
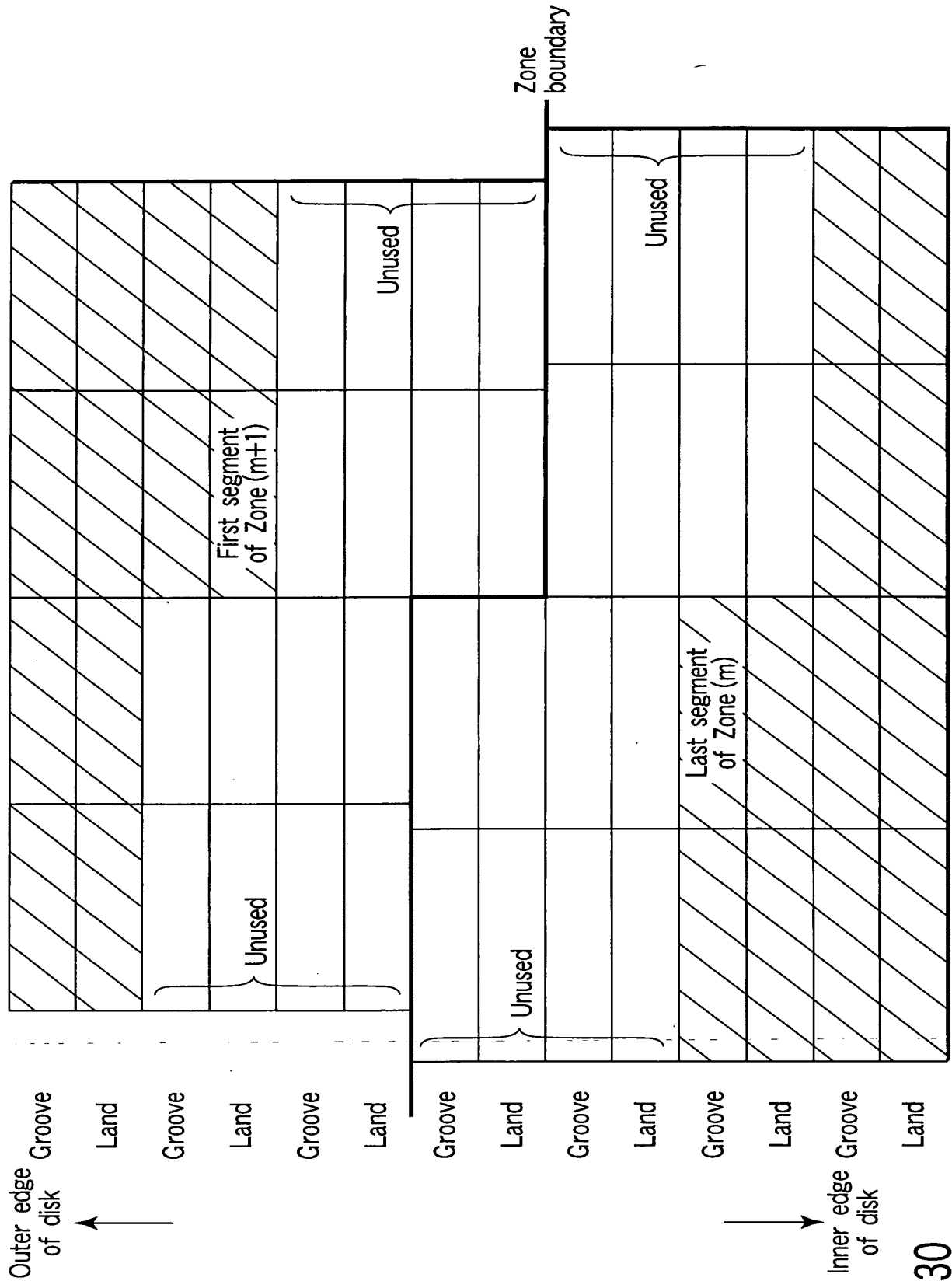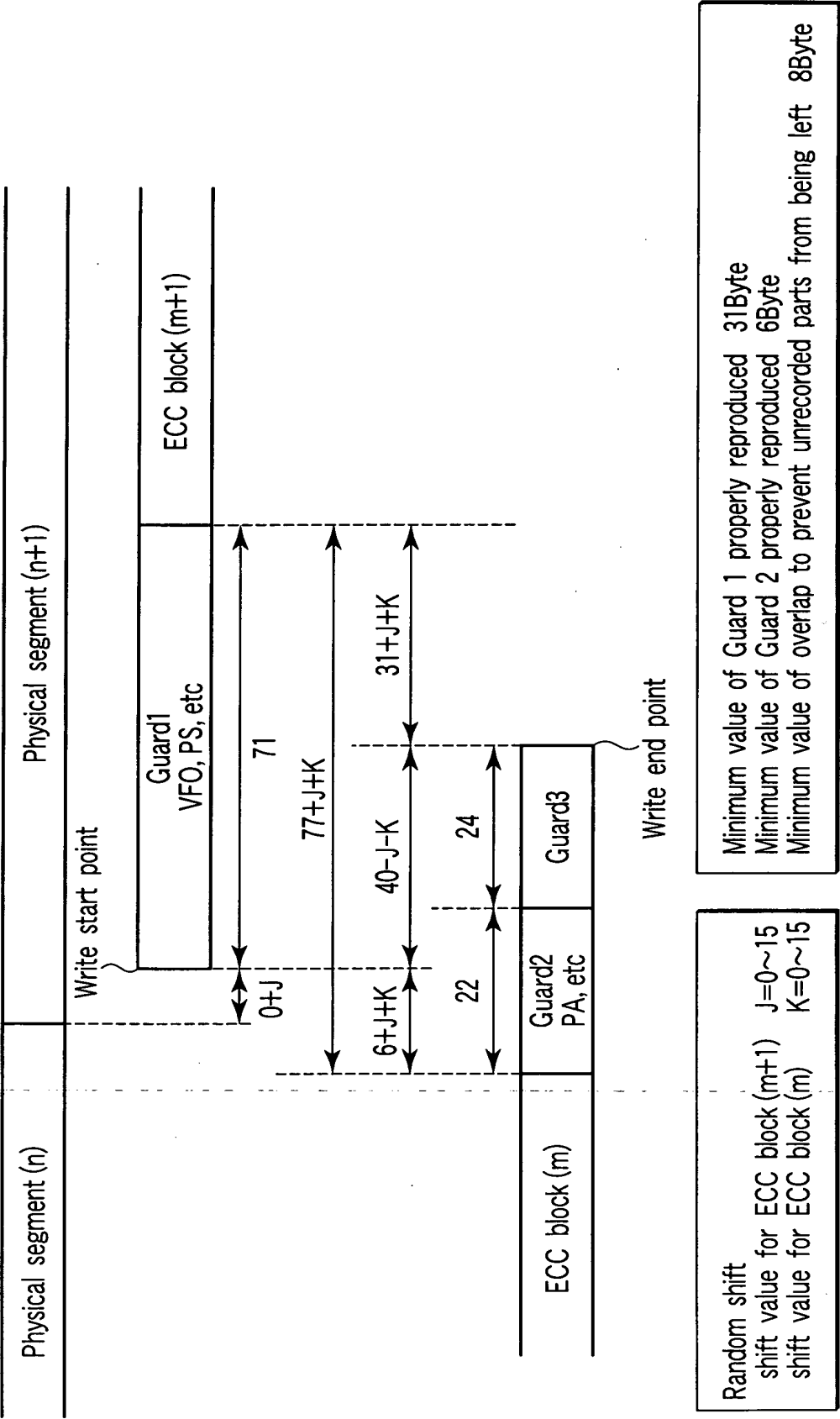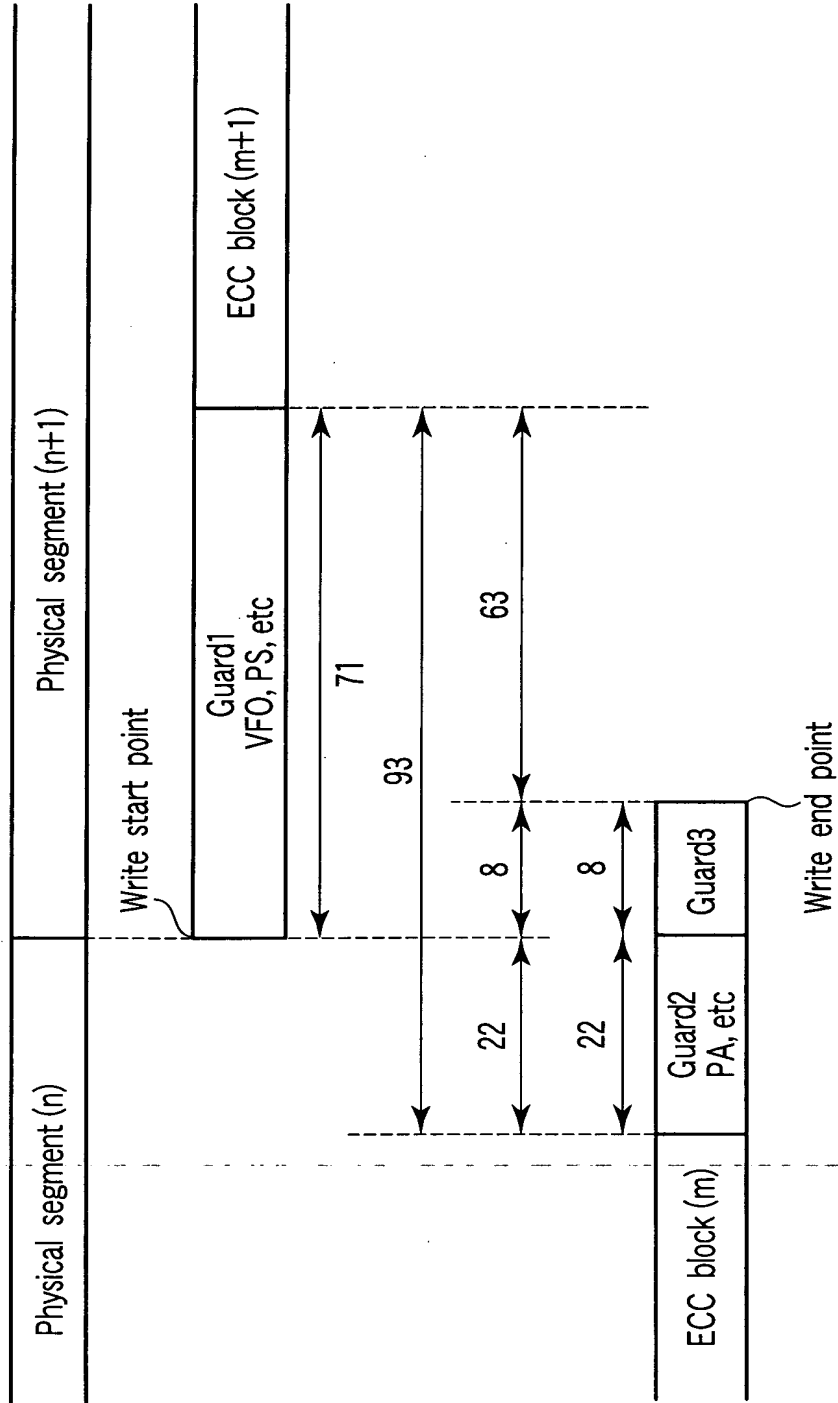
Guard 1 properly reproduced contains 47 bytes
Guard 2 properly reproduced contains 22 bytes
Overlap to prevent unrecorded parts from being left contains 8 bytes
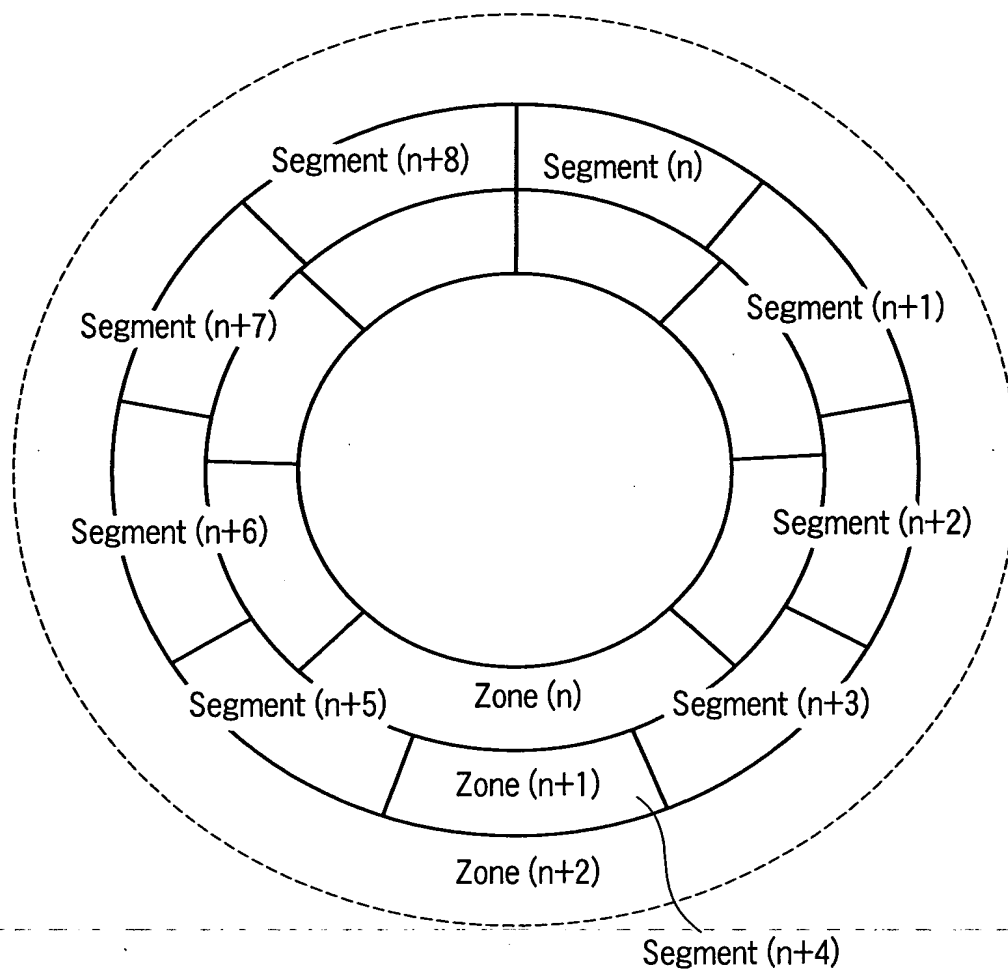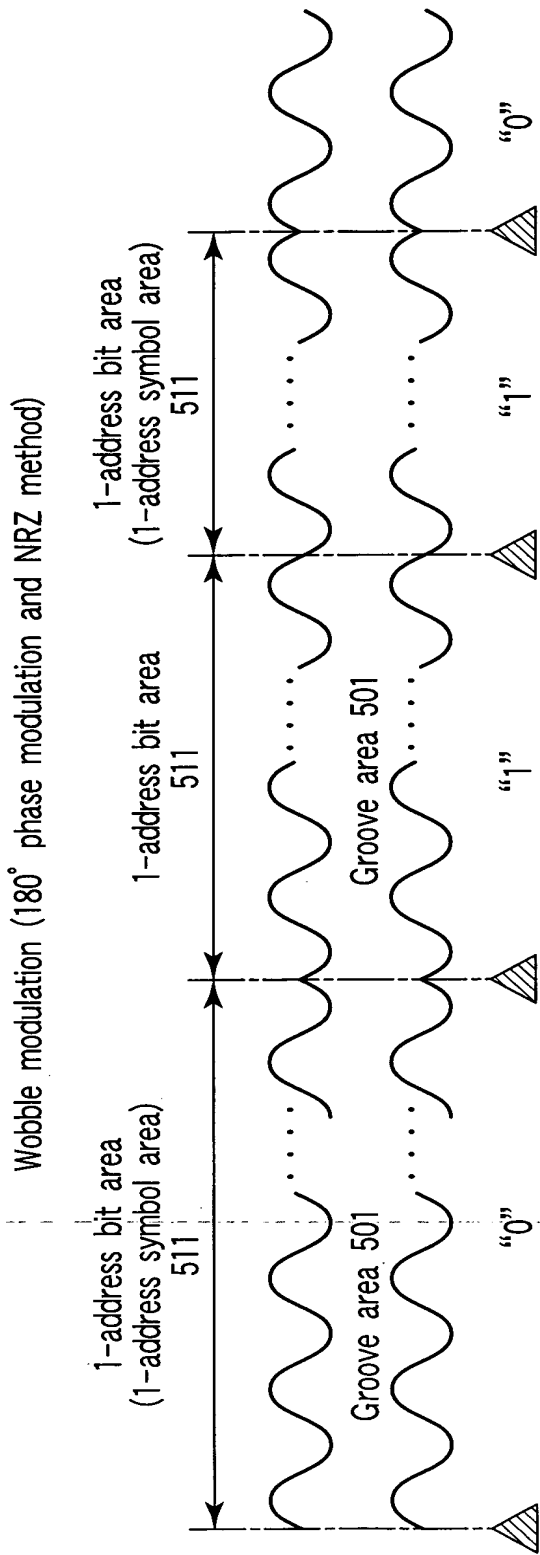
F I G. 32

Segment (n+8) Segment (n)

Segment (n+7)

Segment (n+1)

Segment (n+6)

Segment (n+2)

Segment (n+5) Zone (n) Segment (n+3)

Zone (n+1)

Zone (n+2)

Segment (n+4)

F I G. 33

Wobble modulation (180° phase modulation and NRZ method)

| 1-address bit area (1-address symbol area) 511 | 1-address bit area 511 | 1-address bit area 511 | 1-address bit area (1-address symbol area) 511 |

Groove area 501

Groove area 501

"0"   "1"   "1"   "0"

☆ 1-address bit area 511 (expressed in 8 wobbles or 12 wobbles)
☆ Frequency, amplitude, and phase in 1-address bit area = constant everywhere
☆ Boundary part of 1-address bit area 511 (180° or 0° phase shift)

FIG. 34

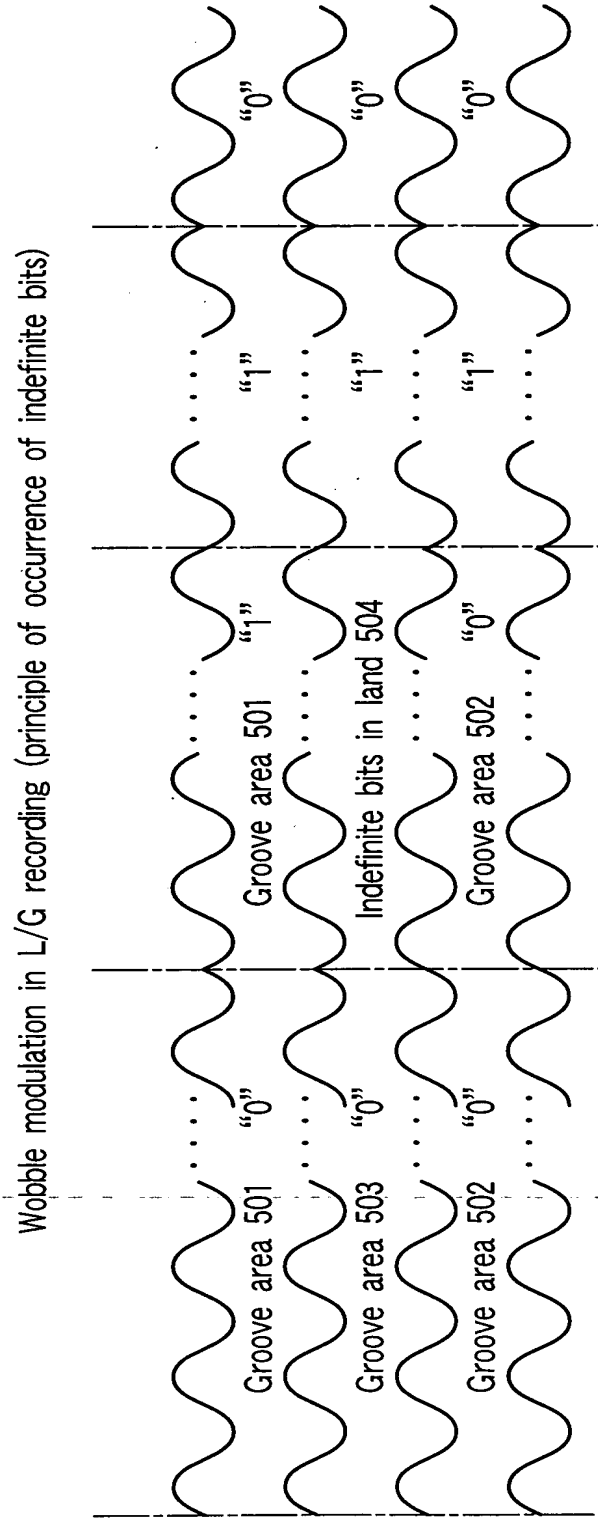Wobble modulation in L/G recording (principle of occurrence of indefinite bits)

Groove area 501 "0"

Groove area 503 "0"

Groove area 502 "0"

Groove area 501 "1"

Indefinite bits in land 504

Groove area 502 "0"

"1" "0"

"1" "0"

"1" "0"

F I G. 35

Example of Gray code

Decimal number	Conventional binary representation	Gray code representation
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

F I G. 36

(Configuration of information recording and reproducing apparatus) (particularly centering on the recording system)

Data ID generating section 165

Interface section 142

Data ID, IED, Data Type, Preset Data, CPR_MAI, EDC adding circuit 168

CPR_MAI data creating section 167

ECC encoding circuit 161

Scramble circuit 157

Data arrangement partial replacement circuit 163

Preset Data creating section 166

Modulation conversion table recording section 153

Modulation circuit 151

DSV computing section 148

SYNC code selecting section 146

SYNC code select table recording section 147

Control section 143

Data combining section 144
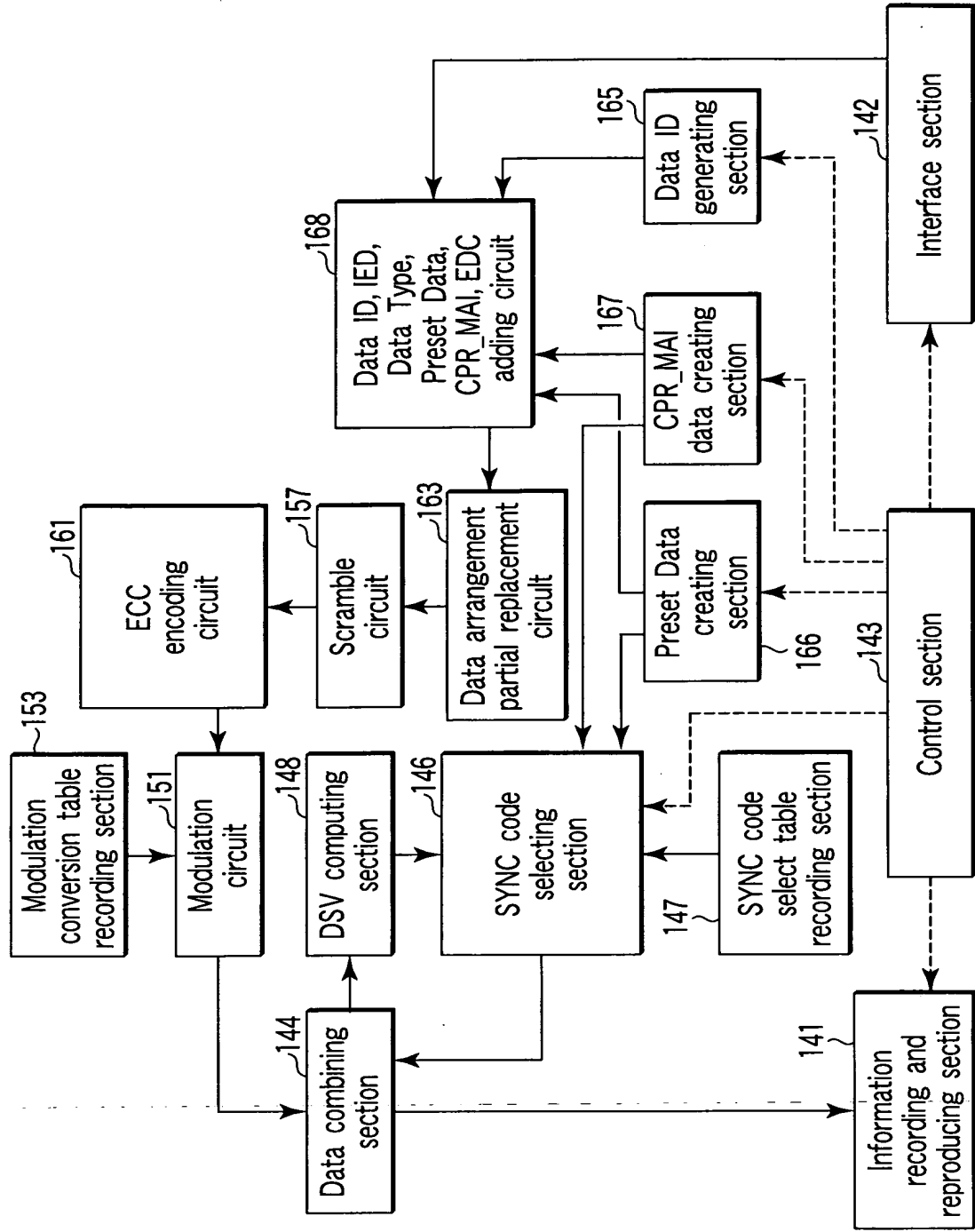
Information recording and reproducing section 141

F I G. 37

(Configuration of information recording and reproducing apparatus) (particularly centering on the reproducing system)

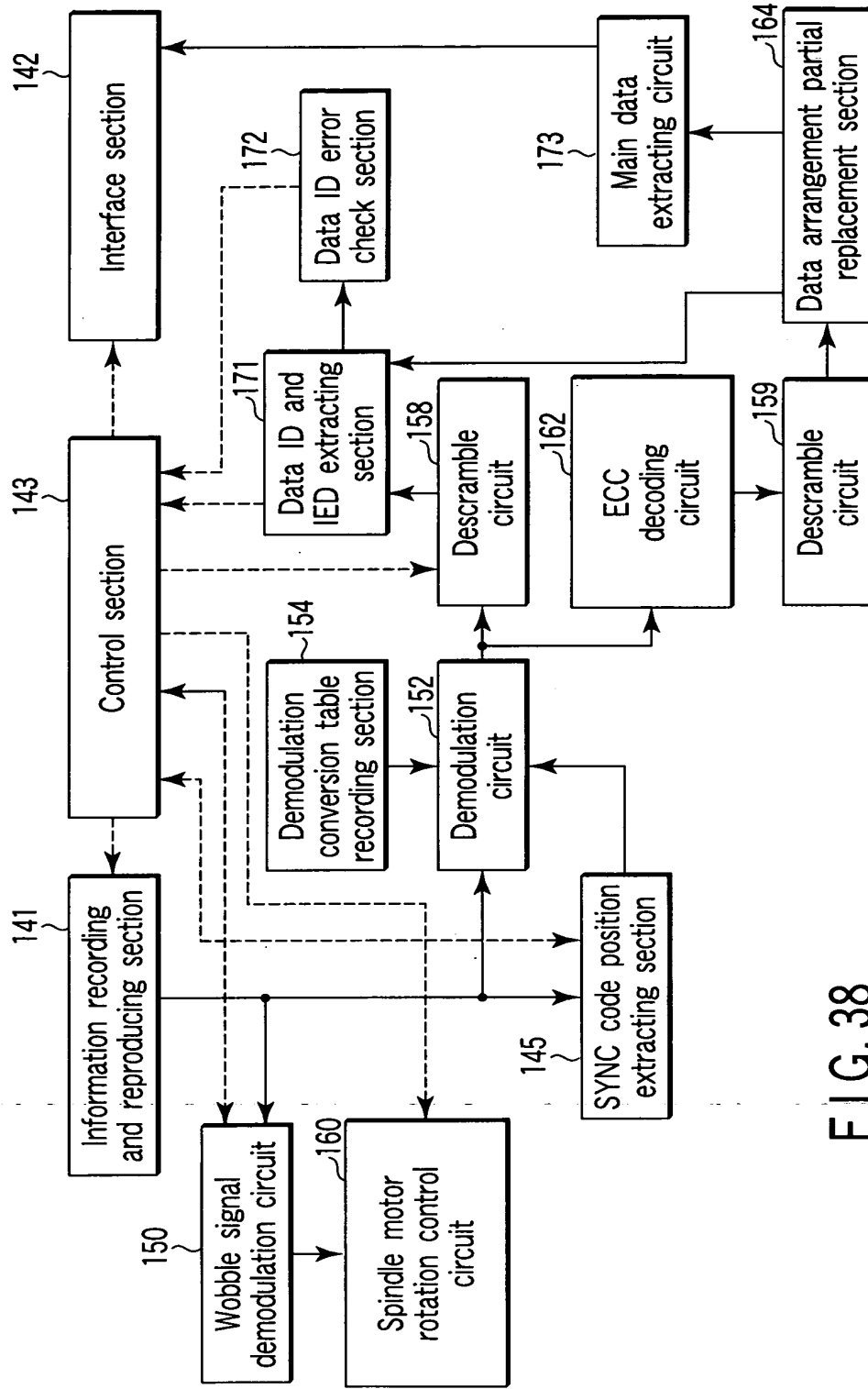Interface section 142

Control section 143

Information recording and reproducing section 141

Data ID error check section 172

Data ID and IED extracting section 171

Demodulation conversion table recording section 154

Descramble circuit 158

ECC decoding circuit 162

Descramble circuit 159

Main data extracting circuit 173

Data arrangement partial replacement section 164

Demodulation circuit 152

SYNC code position extracting section 145

Wobble signal demodulation circuit 150

Spindle motor rotation control circuit 160

F I G. 38